A Suggested Approach for Layout Versus Schematic (LVS) Comparison Using Guardian LVS

Introduction

Different approaches exist to achieve an LVS clean design, and the steps required are often design-dependant. For instance, the differences in device count between the schematic and layout netlists, the difference in netlist structures and the difference of device parameter details may all play a role on how the LVS comparison criteria should be set. This application note describes different practices and tool features, which should facilitate the LVS comparison of a design using the Guardian LVS tool.

It will be noted that the Guardian LVS tool can be used to compare two netlists; Schematic Versus Schematic (SVS), Layout Versus Layout (LVL) and Layout Versus Schematic (LVS). For the purposes of simplicity, the latter situation (LVS) is assumed throughout this application note.

Bottom up Approach

As a general rule, in order to facilitate the LVS process, it is recommended that the LVS comparison be started with the lower level cells in hierarchy and to build its way up in the hierarchy tree of the project. Applying this basic rule will help to smooth the LVS process. This is because when the user compares the higher hierarchy level cells, the LVS errors found will most likely be caused by the connections between the instances, as all of them are known to be LVS clean with their schematic equivalent. This structured approach may seem longer to apply, but it could save many hours of LVS debugging.

Use of Labels

Another good practice is the use of the same net labels in front end (schematic) and back end (layout) design. If all nets getting in and out of a cell are identically labeled in both netlists, it simplifies the debugging task and allows the use of the “Match same name nets” option, found in Setup>>Project Settings…under the tab “General”. Similarly, the designer could name the instances and subcircuits the same and take advantage of the “Match same name devices/instances” and “Match same name subcircuits”.

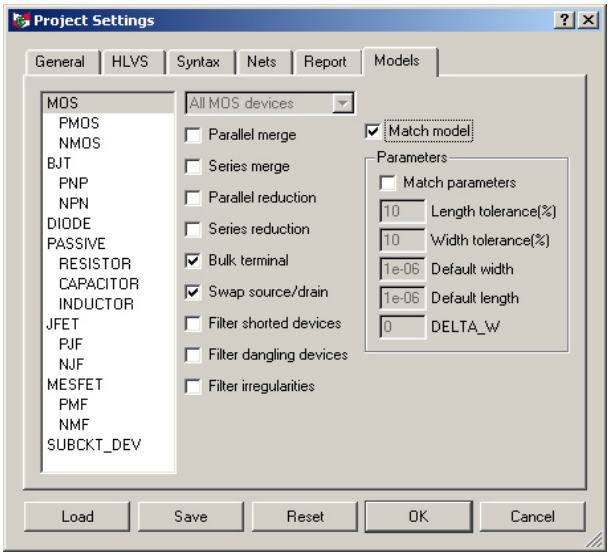

Figure 1: LVS setting without reduction.

Power and Ground Nets

In order to facilitate the LVS process, it is recommended that the power and ground nets for both netlists be specified. To list them, simply fill in the fields found in Setup>>Project Settings…under the tab “Nets”.

Know What you are Comparing

For many basic cells, the device count in the front end and back end netlist is the same. For example, a simple inverter may contain one NMOS and one PMOS in both the front end and back end netlist. In this type of situation, the LVS tool does not need to perform any reduction on the netlists (series merge, parallel merge, series reduction, parallel reduction) to be able to achieve LVS clean. Accordingly, if the two netlists being compared do have a one on one correspondence of device, it is recommended that the first LVS run be set without allowing any reduction during the LVS process, as shown in Figure 1. These settings can be found under Setup>>Project Settings… under the tab “Models”.

If the netlists being compared have a different device count, some reduction or merging will need to be performed on the netlists to find a correspondence. The main aspect to keep in mind, when allowing reduction, is that some nets will collapse in the reduction process. If some of the nets are important and need to remain in the reduced version of the netlist, they should be listed in the "Non-Collapsible Nets" section found in Setup>>Project Settings…under the tab "Nets". The setting for the "Collapsible Nets" can be found at Setup>>Project Settings… under the tab "Syntax".

Setting Matching Criteria Accordingly

As mentioned previously, the matching criteria will be design dependent. But, initially, it is recommended that the criteria be set loosely. The first goal should be to achieve a "connectivity LVS clean". In other words, the electrical connections linking the different devices in the front end should be equivalent to the electrical connections in the back end design; the two netlists should be topologically equivalent. At this stage, the matching criteria do not include the correspondence of device parameters like W and L of resistors, MOS devices or the capacitance value of capacitors. The matching criteria are found under Setup>>Project Settings… under the Tab "Models". Figure 2 illustrates the setting that could be used for the resistors comparison. In this particular case, only the "Match model" box, on the right side, is checked. Therefore, the LVS algorithm will not compare the values nor the W and L of the resistors, but will rather verify if the resistors being compared are of the same model type and if their electrical connections to the rest of the circuitry are equivalent.

Each device type, listed on the left side of Figure 2, has a similar setting, so very conservative settings are recommended for the initial LVS run.

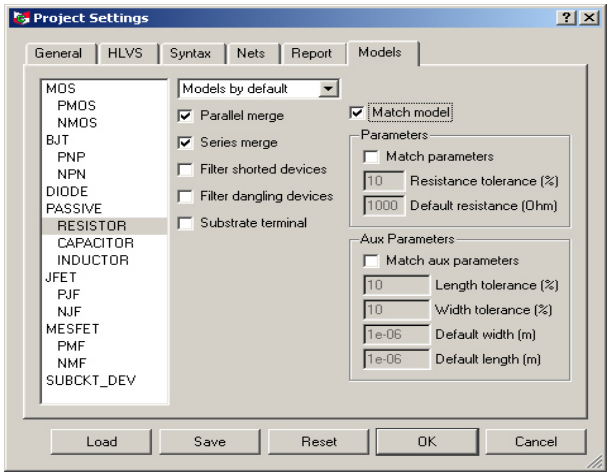

Figure 2: Model matching.

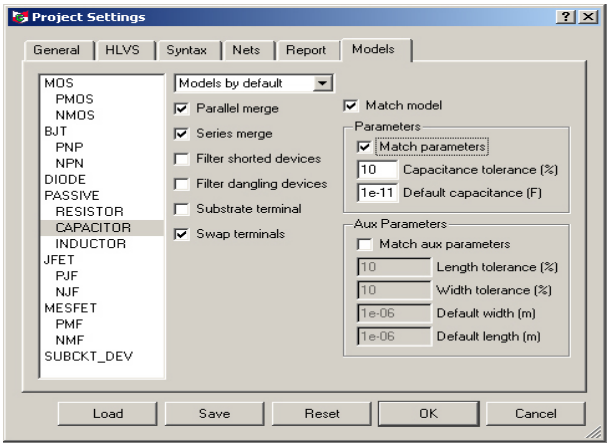

Figure 3: Parameters matching.

It will be noted that, on completion of this stage, the report of the LVS tool will indicate that the two netlists are equivalent. The user should keep in mind that the netlists are equivalent based on the matching criteria that were set, which, at this stage, do not include parameters matching.

Tightening Matching Criteria

Once the "connectivity LVS clean" is achieved, the matching criteria should be tightened to ensure that the back end netlist (layout) is an accurate representation of the front end netlist of the design.

Figure 3 illustrates how the criteria could be set to add the parameter matching for the capacitors. Note that, similarly to the resistors, we can set the Parameters and Aux Parameter separately.

If a specific model requires a different matching, the criteria can be set on a per-model basis. For example, assuming that a PMOS device named "hv_pmos" requires a 5% L and W tolerance instead of the 10% required by all other MOS models, the settings could be as shown in Figure 4.

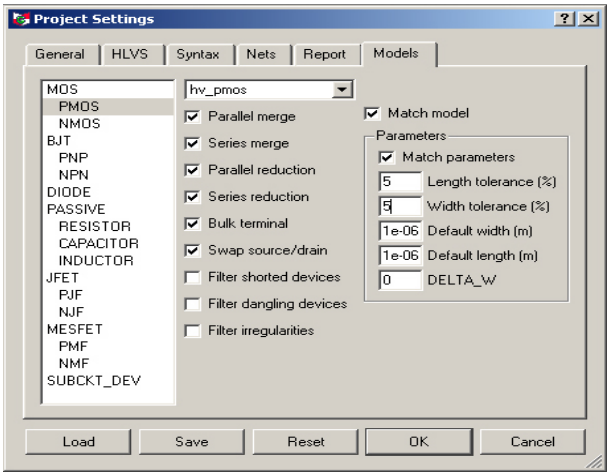

Figure 4: Model-based setting.

Reading the Report

On completion of an LVS comparison, many reports can be generated to assist the user in achieving an LVS clean design. The list of reports can be found under Setup>>Project Setting… under the tab “Report”. For the first few runs, generating all reports is recommended, as it is still uncertain, at this stage, which one could contain the most valuable information.

The first report to be displayed, after completion, is the Active Log File (LO), which is illustrated in Figure 5. This message file indicates if the LVS comparison was successful or not. Three different messages can appear at the top; netslits are equivalent, netlists are not equivalent, or netlists are topologically equivalent but parameter errors exist.

The results displayed in Figure 5 indicate that the two netlists are not equivalent. As no device reduction was allowed in the setting, the before and after preprocessing columns indicate the same device count. The unmatched and matched columns indicate that the discrepancy resides in the number of nets. 41 of the 42 nets in the schematic netlist were match to 41 of the 43 nets of the back end netlist. In order to resolve the net mismatch, it is useful to look at the results of a second report called the Unmatch Report (UM). This report will list the discrepancies and some potential matches.

The UM report shown in Figure 6 indicates that the net TRA48:Q0 of the first netlist could possibly match with net TRA48:#20 of the second netlist. The report also suggests that net TRA48:Q0 could be match with TRA48:Q0 of the second netlist. In this case, it is useful to look at the stats line located below the recommend match. The first line, “stats: 12/2 - 0/0 - 10/0 – 2” indicates that there is a total of 12 connections to net TRA48:Q0 in the first netlist and that, if we were to match these two nets, 10 of the 12 connections in the first netlist would be in disagreement with this match. It also illustrates that there is a total of 2 connections to net TRA48:#20 in the second netlist and the two connections would be in agreement with this match.

The second stats line “stats: 12/10 – 0/0 – 2/0 – 10” indicates that there is a total of 10 connections to net TRA48:Q0 in the second netlist and that matching these

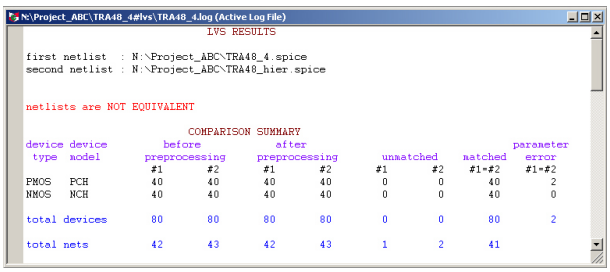
N:\Project_ABC\TRA48_4#lvs\TRA48_4.log (Active Log File)
LVS RESULTS
first netlist : N:\Project_ABC\TRA48_4.spice
second netlist : N:\Project_ABC\TRA48_hier.spice
netlists are NOT EQUIVALENT
COMPARISON SUMMARY
device type model
device before preprocessing #1 #2
device after preprocessing #1 #2
unmatched #1 #2
matched #1=#2
parameter error #1=#2
PMOS PCH 40 40 40 40 0 0 40 2
NMOS NCH 40 40 40 40 0 0 40 0
total devices 80 80 80 80 0 0 80 2
total nets 42 43 42 43 1 2 41

Figure 5. Active Log File.

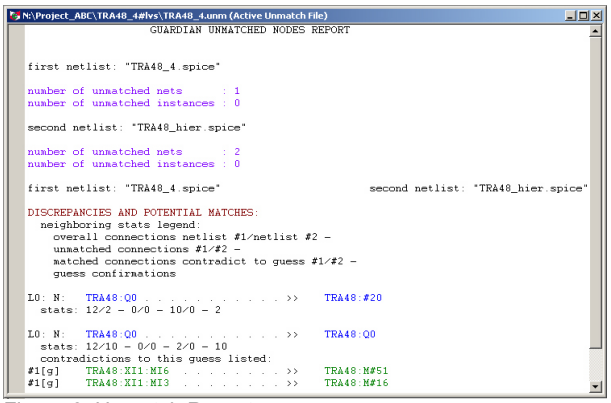
N:\Project_ABC\TRA48_4#lvs\TRA48_4.unm (Active Unmatch File)
GUARDIAN UNMATCHED NODES REPORT
first netlist: "TRA48_4.spice"
number of unmatched nets : 1
number of unmatched instances : 0
second netlist: "TRA48_hier.spice"
number of unmatched nets : 2
number of unmatched instances : 0
first netlist: "TRA48_4.spice" second netlist: "TRA48_hier.spice"
DISCREPANCIES AND POTENTIAL MATCHES:
neighboring stats legend:
overall connections netlist #1/netlist #2 –
unmatched connections #1/#2 –
matched connections contradict to guess #1/#2 –
guess confirmations
L0: N: TRA48:Q0 >> TRA48:#20
stats: 12/2 – 0/0 – 10/0 – 2
L0: N: TRA48:Q0 >> TRA48:Q0
stats: 12/10 – 0/0 – 2/0 – 10
contradictions to this guess listed:
#1[g] TRA48:XI1:MI6 >> TRA48:M#51
#1[g] TRA48:XI1:MI3 >> TRA48:M#16

Figure 6. Unmatch Report.

two nets would lead to a guess confirmations of 10. In this specific case, we can intuitively deduct that the sum of two TRA48:#20 nets and ten TRA48:Q0 nets in the second netlist totaled to 12 nets. Therefore, the net is most likely broken between the TRA48:Q0 and TRA48:#20 leaving two connections unconnected to the main net TRA48:Q0.

To confirm this assumption, we can cross probe the net listed in this report and inspect them in the layout. By simply double clicking the net TRA48:#20, a pop up window will open, allowing the user to select LVS Navigator (see Figure 7). When pressing OK, the net will be high-

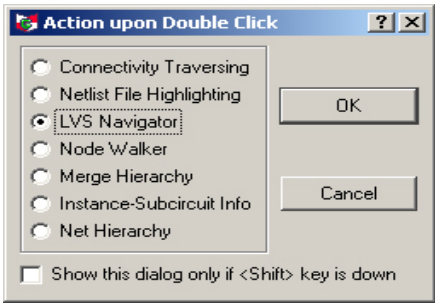

Figure 7. Action upon Double Click.

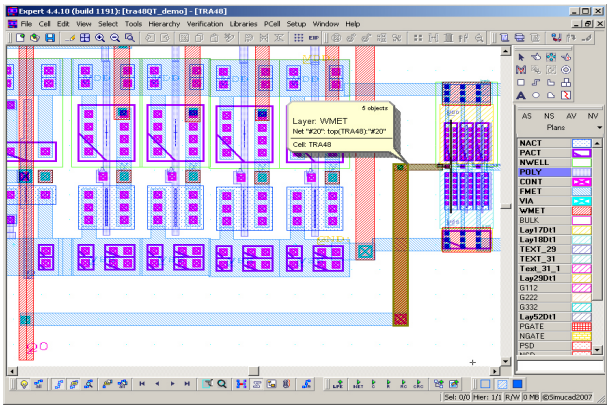

Figure 8: Cross Probing first net.

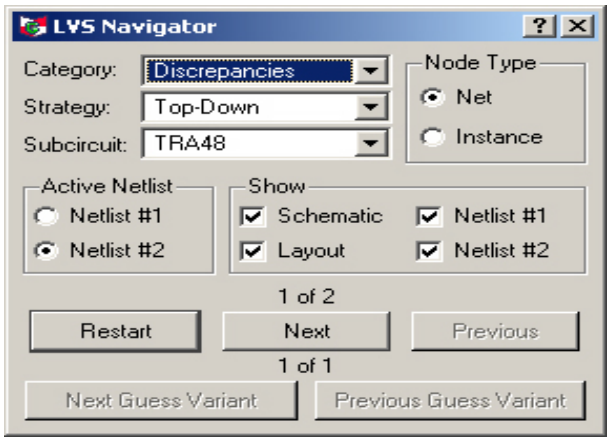

Figure 9: LVS Navigator.

lighted in Expert as shown in Figure 8.

To scroll through the nets, simply press “Next” in the LVS navigator window illustrated in Figure 9 and the second part of the suggested match will be highlighted in the Layout window. Figure 10 clearly displays that the net is broken in the bottom right corner of the visible layout area.

After correcting this layout error, a second LVS run was performed. On completion of this run, the Active Log window, shown in Figure 11, indicates that the netlists are topologically equivalent but some parameter errors (PE) exist. The last column of the log file shows that the PE exists for the PMOS device.

The PE report (see Figure 12) will be useful in order to investigate this claim. This report lists all mismatches of parameters between the first netlist devices, located to the left, and the second netlist devices. As indicated, the back end PMOS device M#68 has a width of 4.6u instead of the 4u value found for the equivalent device in the front end netlist. The user can utilize the LVS Navigator feature to find both PMOS devices in the layout,

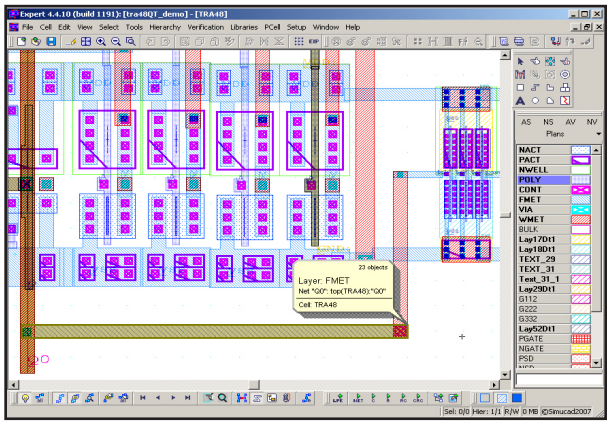

Figure 10: Cross Probing second net

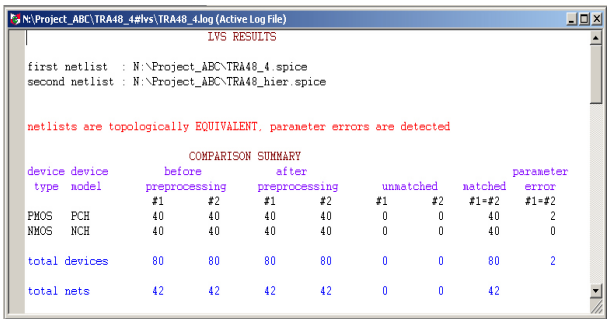
N:\Project_ABC\TRA48_4#lvs\TRA48_4.log (Active Log File)
LVS RESULTS
first netlist : N:\Project_ABC\TRA48_4.spice
second netlist : N:\Project_ABC\TRA48_hier.spice
netlists are topologically EQUIVALENT, parameter errors are detected
COMPARISON SUMMARY
device type model
before preprocessing #1 #2
after preprocessing #1 #2
unmatched #1 #2
matched #1=#2
parameter error #1=#2
PMOS PCH 40 40 40 40 0 0 40 2
NMOS NCH 40 40 40 40 0 0 40 0
total devices 80 80 80 80 0 0 80 2
total nets 42 42 42 42 0 0 42

Figure 11: Active Log topologically equivalent.

and correct their width to match the parameter listed in the first netlist.

Other reports are available, and chapter 4, section 5 of the *Guardian Layout Verification User’s Manual* explains more about their use.

Useful Debugging Tools

Different tools features can assist the user throughout the debugging process. In addition to the previously discussed LVS Navigator, which highlights the nets in Expert Layout Editor, Guardian LVS also allows the cross probing between the Layout (Expert) and Schematic tool (Gateway). From within Guardian LVS, under the menu “Action,” the user can select “Launch Gateway” or “Launch Gateway Views.” In this Gateway session, if the schematic corresponding to the front end netlist is open, the LVS Navigator feature will now highlight the nets in both netlists, in the layout, and in the schematic tool.

Finally, some useful features are made available in the Expert layout editor tool. Expert offers three different features that may be of a great assistance in order to resolve any LVS mismatch, the “Node probing”, the “Net and device search” and the “Short locator”. More about these features can be found in the *Expert Layout Editor User’s Manual*.

Conclusion:

This application note has described different practices and tool features that should reduce the time required to

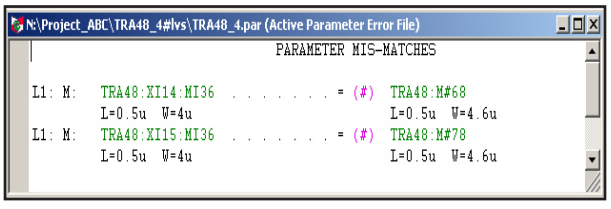
N:\Project_ABC\TRA48_4#lvs\TRA48_4.par (Active Parameter Error File)
PARAMETER MIS-MATCHES
L1: M: TRA48:XI14:MI36 . . . . . = (#) TRA48:M#68
L=0.5u W=4u L=0.5u W=4.6u
L1: M: TRA48:XI15:MI36 . . . . . = (#) TRA48:M#78
L=0.5u W=4u L=0.5u W=4.6u

Figure 12: Parameter Error Report.